$$f = X_n \overset{n-1}{\underset{1}{\Xi}} X_k + X_n' (\overset{n-1}{\underset{1}{\Xi}} X_k)' = (\overset{n}{\underset{1}{\Xi}} X_k)' .$$

From the symmetry of this function there is no other way of expanding which will reduce the number of elements. If the functions are substituted in the other order we get

$$f = X_n (\overset{n-1}{\underset{1}{\Xi}} X_k)' + X_n' \overset{n-1}{\underset{1}{\Xi}} X_k = \overset{n}{\underset{1}{\Xi}} X_k .$$

This completes the proof that these functions require the most elements.

To show that each requires $(3 \cdot 2^{n-1} - 2)$ elements, let the number of elements required be denoted by $s(n)$. Then from (19) we get the difference equation

$$s(n) = 2s(n-1) + 2 ,$$

with $s(2) = 4$. This is linear, with constant coefficients, and may be solved by the usual methods. The solution is

$$s(n) = 3 \cdot 2^{n-1} - 2 ,$$

as may easily be verified by substituting in the difference equation and boundary condition.

Note that the above only applies to a series-parallel realization. In a later section it will be shown that the function $\overset{n}{\underset{1}{\Xi}} X_k$ and its negative may be realized with $4(n-1)$ elements using a more general type of circuit. The function requiring the most elements using any type of circuit has not as yet been determined.

Dual Networks

The negative of any network may be found by De Morgan's theorem, but the network must first be transformed into an equivalent series-parallel circuit (unless it is already of this type). A theorem will be developed with which the negative of any planar two-terminal circuit may be found directly. As a corollary a method of finding a constant-current circuit equivalent to a given constant-voltage circuit and vice versa will be given.

Let N represent a planar network of hindrances, with the function X_{ab} between the terminals a and b which are on the outer edge of the network. For definiteness consider the network of Figure 15 (here the hindrances are shown merely as lines).

Now let M represent the dual of N as found by the following process; for each contour or mesh of N assign a node or junction point of M. For each element of N, say X_k, separating the contours r and s there corresponds an element X_k' connecting the nodes r and s of M. The area exterior to N is to be considered as two meshes, c and d, corresponding to nodes c and d of M. Thus the dual of Figure 15 is the network of Figure 16.

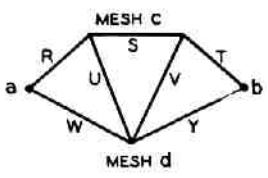

Figure 15 (left). Planar network for illustration of duality theorem

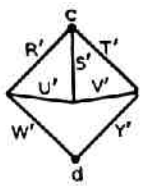

Figure 16 (right). Dual of figure 15

Theorem: If M and N bear this duality relationship, then $X_{ab} = X'_{cd}$. To prove this, let the network M be superimposed upon N, the nodes of M within the corresponding meshes of N and corresponding elements crossing. For the network of Figure 15, this is shown in Figure 17 with N solid and M dotted. Incidentally, the easiest method of finding the dual of a network (whether of this type or an impedance network) is to draw the required network superimposed on the given network. Now, if $X_{ab} = 0$, then there must be some path from a to b along the lines of N such that every element on this path equals zero. But this path represents a path *across* M dividing the circuit from c to d along which every element of M is one. Hence $X_{cd} = 1$. Similarly, if $X_{cd} = 0$, then $X_{ab} = 1$, and it follows that $X_{ab} = X'_{cd}$.

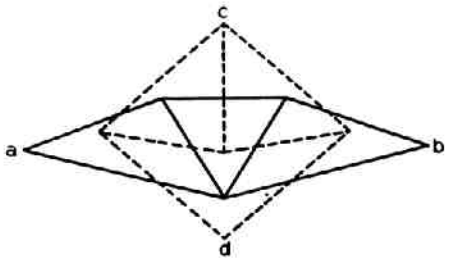

Figure 17. Superposition of a network and its dual

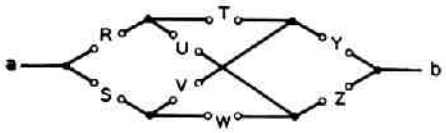

Figure 18. Nonplanar network

It is evident from this theorem that a negative for any planar network may be realized with the same number of elements as the given network.†

In a constant-voltage relay system all the relays are in parallel across the line. To open a relay a series connection is opened. The general constant-voltage system is shown in Figure 19. In a constant-current system the relays are all in series in the line. To de-operate a relay it is short-circuited. The general constant-current circuit corresponding to Figure 19 is shown in Figure 20. If the relay Y_k of Figure 20 is to be operated whenever the relay X_k of Figure 19 is operated and not otherwise, then evidently the hindrance in parallel with Y_k which short-circuits it must be the negative of the hindrance in series with X_k which connects it across the voltage source. If this is true for all the relays, we shall say that the constant-current and constant-voltage systems are equivalent. The above theorem may be used to find equivalent circuits of this sort, for if we make the networks N and M of Figures 19 and 20 duals in the sense described, with X_k and Y_k as corresponding elements, then the condition will be satisfied. A simple example of this is shown in Figures 21 and 22.

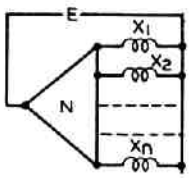

Figure 19 (left). General constant-voltage relay circuit

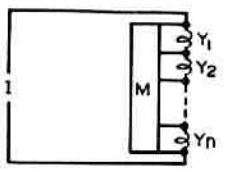

Figure 20 (right). General constant-current relay circuit

† This is not in general true if the word "planar" is omitted. The nonplanar network X_{ab}, of Figure 18, for example, has no negative containing only eight elements.

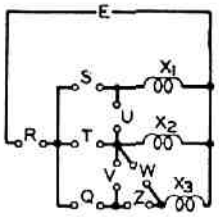

Figure 21 (left). Simple constant-voltage system

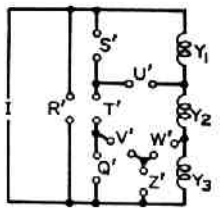

Figure 22 (right). Constant-current system equivalent to figure 21

Synthesis of the General Symmetric Function

It has been shown that any function represents explicitly a series-parallel circuit. The series-parallel realization may require more elements, however, than some other network representing the same function. In this section a method will be given for finding a circuit representing a certain type of function which in general is much more economical of elements than the best series-parallel circuit. This type of function is known as a symmetric function and appears frequently in relay circuits.

Definition: A function of the n variables $X_1, X_2 \ldots X_n$ is said to be symmetric in these variables if any interchange of the variables leaves the function identically the same. Thus $XY + XZ + YZ$ is symmetric in the variables X, Y, and Z. Since any permutation of variables may be obtained by successive interchanges of two variables, a necessary and sufficient condition that a function be symmetric is that any interchange of two variables leaves the function unaltered.

By proper selection of the variables many apparently unsymmetric functions may be made symmetric. For example, $XY'Z + X'YZ + X'Y'Z'$ although not symmetric in X, Y, and Z is symmetric in X, Y, and Z'. It is also sometimes possible to write an unsymmetric function as a symmetric function multiplied by a simple term or added to a simple term. In such a case the symmetric part may be realized with the methods to be described, and the additional term supplied as a series or parallel connection.

The following theorem forms the basis of the method of design which has been developed.

Theorem: A necessary and sufficient condition that a function be symmetric is that it may be specified by stating a set of numbers $a_1, a_2 \ldots a_k$ such that if exactly $a_j (j = 1,2,3\ldots,)$ of the variables are zero, then the function is zero and not otherwise. This follows easily from the definition. The set of numbers $a_1, a_2 \ldots a_k$ may be any set of numbers selected from the numbers 0 to n inclusive, where n is the number of variables in the symmetric function. For convenience, they will be called the a-numbers of the function. The symmetric function $XY + XZ + YZ$ has the a-numbers 2 and 3, since the function is zero if just two of the variables are zero or if three are zero, but not if none or if one is zero. To find the a-numbers of a given symmetric function it is merely necessary to evaluate the function with $0,1 \ldots n$ of the variables zero. Those numbers for which the result is zero are the a-numbers of the function.

Theorem: There are 2^{n+1} symmetric functions of n variables. This follows from the fact that there are $n + 1$ numbers, each of which may be taken or not in our selection of a-numbers. Two of the functions are trivial, however, namely, those in which all and one of the numbers are taken. These give the "functions" 0 and 1, respectively. The symmetric function of the n variables $X_1, X_2 \ldots X_n$ with the a-numbers $a_1, a_2 \ldots a_k$ will be written $S_{a_1 a_2 \ldots a_k}(X_1, X_2, \ldots, X_n)$. Thus the example given would be $S_{23}(X,Y,Z)$. The circuit which has

been developed for realizing the general symmetric function is based on the a-numbers of the function and we shall now assume that they are known.

Theorem: The sum of two given symmetric functions of the same set of variables is a symmetric function of these variables having for a-numbers those numbers common to the two given functions. Thus $S_{1,2,3}(X_1 \ldots X_6) + S_{2,3,5}(X_1 \ldots X_6) = S_{2,3}(X_1 \ldots X_6)$.

Theorem: The product of two given symmetric functions of the same set of variables is a symmetric function of these variables with all the numbers appearing in either or both of the given functions for a-numbers. Thus $S_{1,2,3}(X_1 \ldots X_6) \cdot S_{2,3,5}(X_1 \ldots X_6) = S_{1,2,3,5}(X_1 \ldots X_6)$.

To prove these theorems, note that a product is zero if either factor is zero, while a sum is zero only if both terms are zero.

Theorem: The negative of a symmetric function of n variables is a symmetric function of these variables having for a-numbers all the numbers from 0 to n inclusive which are not in the a-numbers of the given function. Thus $S'_{2,3,5}(X_1 \ldots X_6) = S_{0,1,4,6}(X_1 \ldots X_6)$.

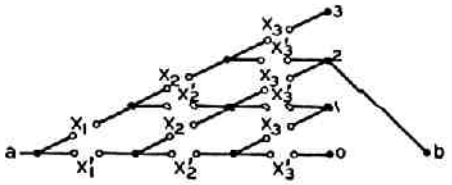

Figure 23. Circuit for realizing $S_2(X_1, X_2, X_3)$

Before considering the synthesis of the general symmetric function $S_{a_1 a_2 \ldots a_i}(X_1, X_2, \ldots, X_n)$ a simple example will be given. Suppose the function $S_2(X_1, X_2, X_3)$ is to be realized. This means that we must construct a circuit which will be closed when any two of the variables X_1, X_2, X_3 are zero, but open if none, or one or three are zero. A circuit for this purpose is shown in Figure 23. This circuit may be divided into three bays, one for each variable, and four levels marked 0, 1, 2 and 3 at the right. The terminal b is connected to the levels corresponding to the a-numbers of the required function, in this case to the level marked 2. The line coming in at a first encounters a pair of hindrances X_1 and X'_1. If $X_1 = 0$, the line is switched up to the level marked 1, meaning that one of the variables is zero; if not it stays at the same level. Next we come to hindrances X_2 and X'_2. If $X_2 = 0$, the line is switched up a level; if not, it stays at the same level. X_3 has a similar effect. Finally reaching the right-hand set of terminals, the line has been switched up to a level equal to the total number of variables which are zero. Since terminal b is connected to the level marked 2, the circuit $a-b$ will be completed if and only if 2 of the variables are zero. If $S_{0,3}(X_1, X_2, X_3)$ had been desired, terminal b would be connected to both levels 0 and 3. In Figure 23 certain of the elements are evidently superfluous. The circuit may be simplified to the form of Figure 24.

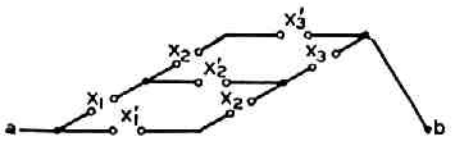

Figure 24. Simplification of figure 23

For the general function exactly the same method is followed. Using the general circuit for n variables of Figure 25, the terminal b is connected to the levels corresponding to the a-

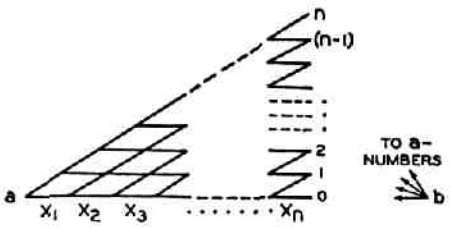

Figure 25. Circuit for realizing the general symmetric function $S_{a_1 a_2 \ldots a_k}(X_1, X_2, \ldots X_n)$

numbers of the desired symmetric function. In Figure 25 the hindrances are respected merely by lines, and the letters are omitted from the circuit, but the hindrance of each line may easily be seen by generalizing Figure 23. After terminal b is connected, all superfluous elements may be deleted.

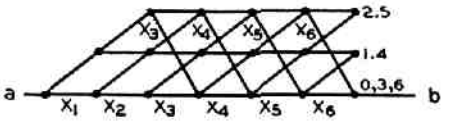

Figure 26. Circuit for $S_{0,3,6}(X_1 \ldots X_6)$ using the "shifting down" process

In certain cases it is possible to greatly simplify the circuit by shifting the levels down. Suppose the function $S_{0,3,6}(X_1 \ldots X_6)$ is desired. Instead of continuing the circuit up to the sixth level, we connect the second level back down to the zero level as shown in Figure 26. The zero level then also becomes the third level and the sixth level. With terminal b connected to this level, we have realized the function with a great savings of elements. Eliminating unnecessary elements the circuit of Figure 27 is obtained. This device is especially useful if the a-numbers form an arithmetic progression, although it can sometimes be applied in other cases.

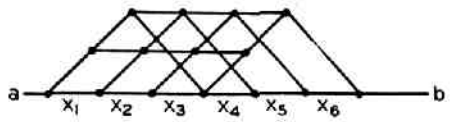

Figure 27. Simplification of figure 26

The functions $\overset{n}{\underset{1}{\Xi}} X_k$ and $(\overset{n}{\underset{1}{\Xi}} X_k)'$ which were shown to require the most elements for a series parallel realization have very simple circuits when developed in this manner. It can be easily shown that if n is even, then $\overset{n}{\underset{1}{\Xi}} X_k$ is the symmetric function with all the even numbers for a-numbers, if n is odd it has all the odd numbers for a-numbers. The function $(\overset{n}{\underset{1}{\Xi}} X_k)'$ is, of course, just the opposite. Using the shifting-down process the circuits are as shown in Figures 28 and 29. These circuits each require $4(n-1)$ elements. They will be recognized as the familiar circuit for controlling a light from n points, using $(n-2)$ double-pole double-throw switches and two single-pole double-throw switches. If at any one of the points the position of the switch is changed, the total number of variables which equal zero is changed by one, so that if the light is on, it will be turned off and if already off, it will be turned on.

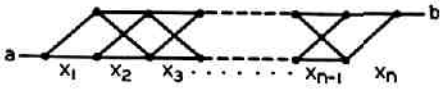

Figure 28. $\overset{n}{\underset{1}{\Xi}} X_k$ for n odd, $\left(\overset{n}{\underset{1}{\Xi}} X_k\right)'$ for n even

More than one symmetric function of a certain set of variables may be realized with just one circuit of the form of Figure 25, providing the different functions have no a-numbers in common. If there are common a-numbers the levels may be shifted down, or an extra relay may be added so that one circuit is still sufficient.

The general network of Figure 25 contains $n(n+1)$ elements. We will show that for any given selection of a-numbers, at least n of the elements will be superfluous. Each number from 1 to $n-1$ inclusive which is not in the set of a-numbers produces two unnecessary elements; 0 or n missing will produce one unnecessary element. However, if two of the a-numbers differ by only one, then two elements will be superfluous. If more than two of the a-numbers are adjacent, or if two or more adjacent numbers are missing, then more than one element apiece will be superfluous. It is evident then that the worst case will be that in which the a-numbers are all the odd numbers or all the even numbers from 0 to n. In each of these cases it is easily seen that n of the elements will be superfluous. In these cases the shifting down process may be used if $n > 2$ so that the maximum of n^2 elements will be needed only for the four particular functions X, X', $X \oplus Y$, and $(X \oplus Y)'$.

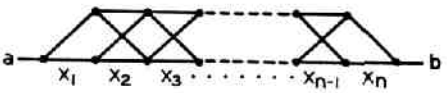

Figure 29. $\left(\overset{n}{\underset{1}{\Xi}} X_k\right)$ for n even, $\left(\overset{n}{\underset{1}{\Xi}} X_k\right)'$ for n odd

Equations From Given Operating Characteristics

In general, there is a certain set of independent variables A, B, C... which may be switches, externally operated or protective relays. There is also a set of dependent variables x, y, z... which represent relays, motors or other devices to be controlled by the circuit. It is required to find a network which gives, for each possible combination of values of the independent variables, the correct values for all the dependent variables. The following principles give the general method of solution.

1. Additional dependent variables must be introduced for each added phase of operation of a sequential system. Thus if it is desired to construct a system which operates in three steps, two additional variables must be introduced to represent the beginning of the last two steps. These additional variables may represent contacts on a stepping switch or relays which lock in sequentially. Similarly each required time delay will require a new variable, representing a time delay relay of some sort. Other forms of relays which may be necessary will usually be obvious from the nature of the problem.

2. The hindrance equations for each of the dependent variables should now be written down. These functions may involve any of the variables, dependent or independent, including the variable whose function is being determined (as, for example, in a lock-in circuit). The